

FIG. 1

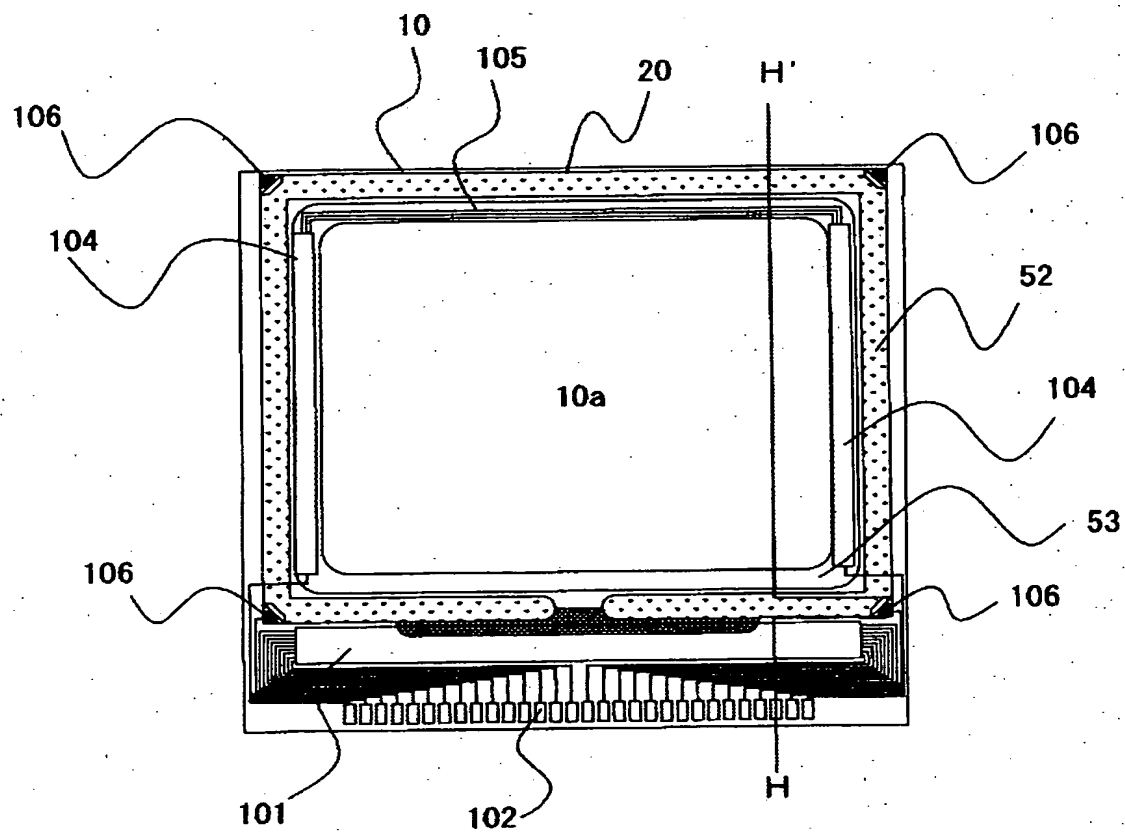


FIG. 2

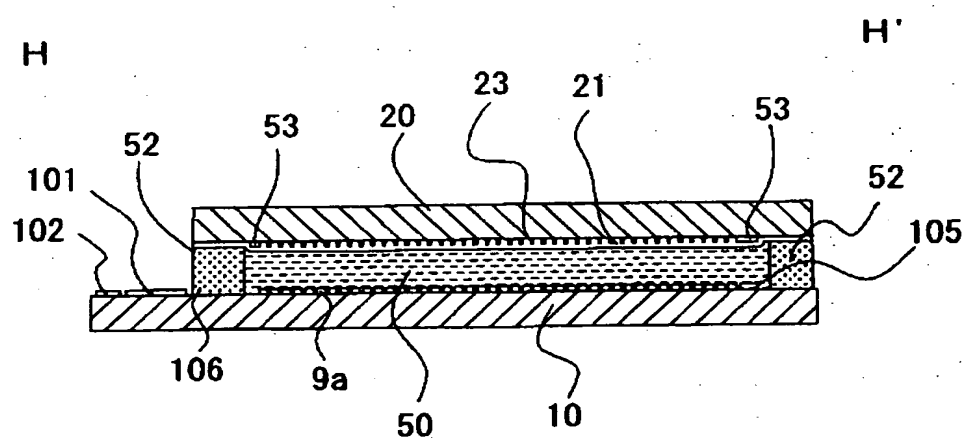


FIG. 3

FIXED POTENTIAL LINE

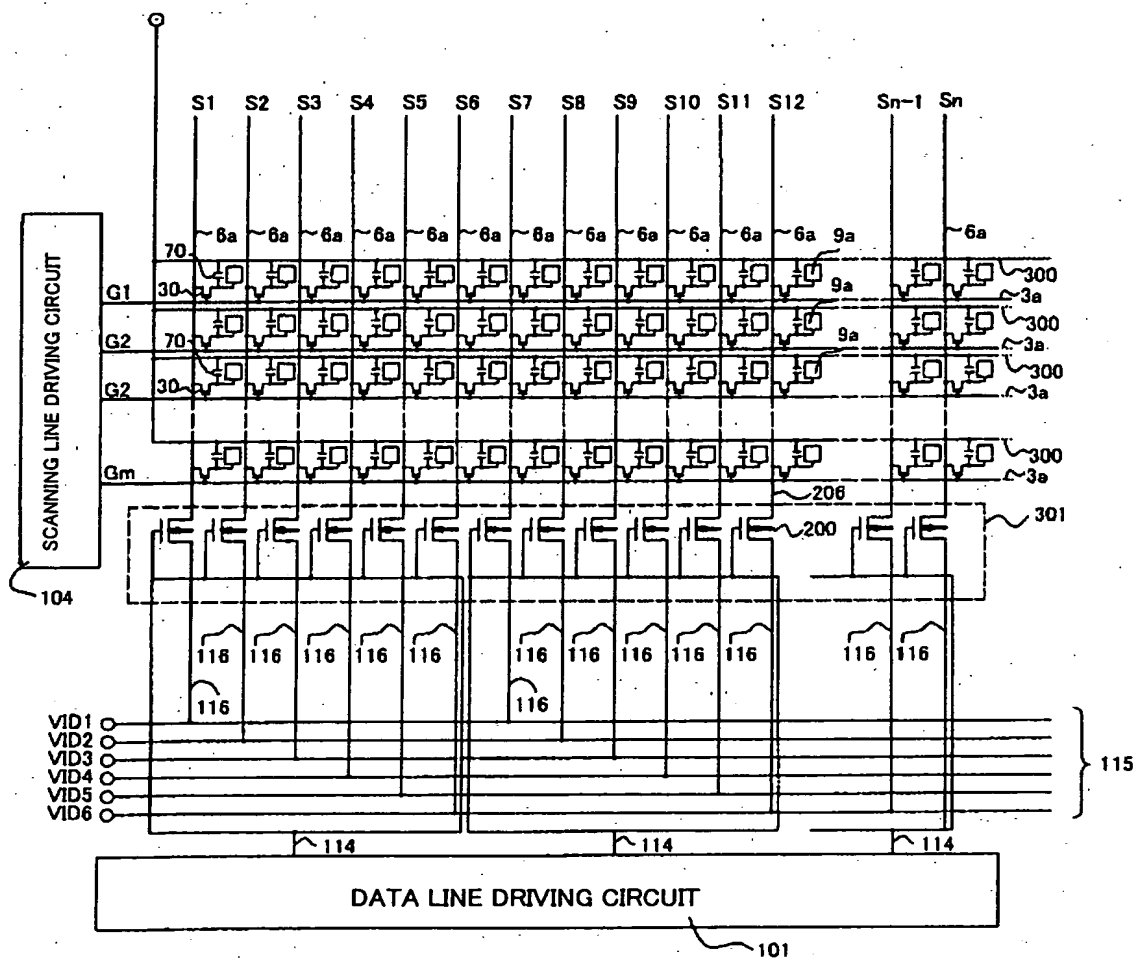


FIG. 4

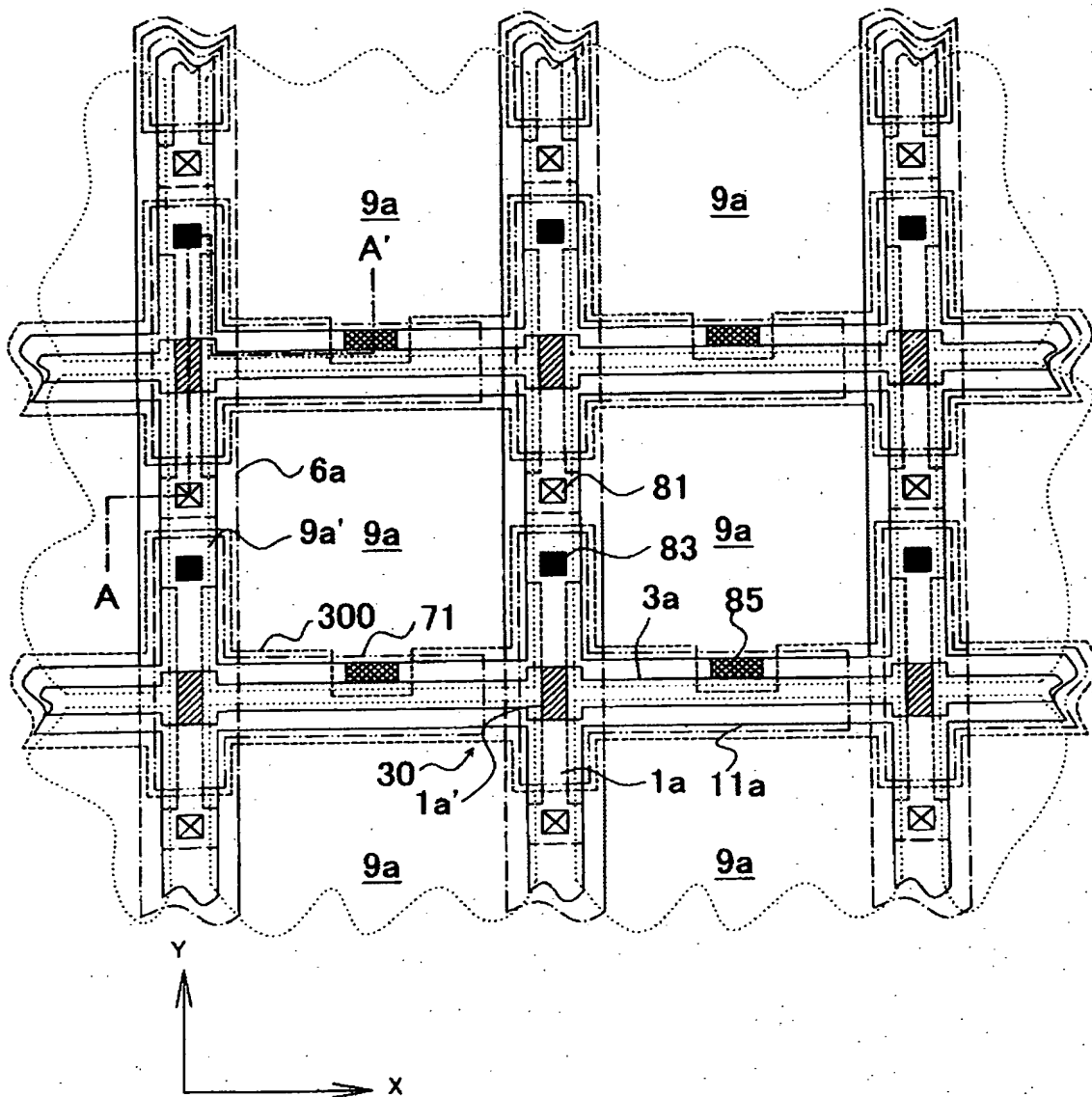
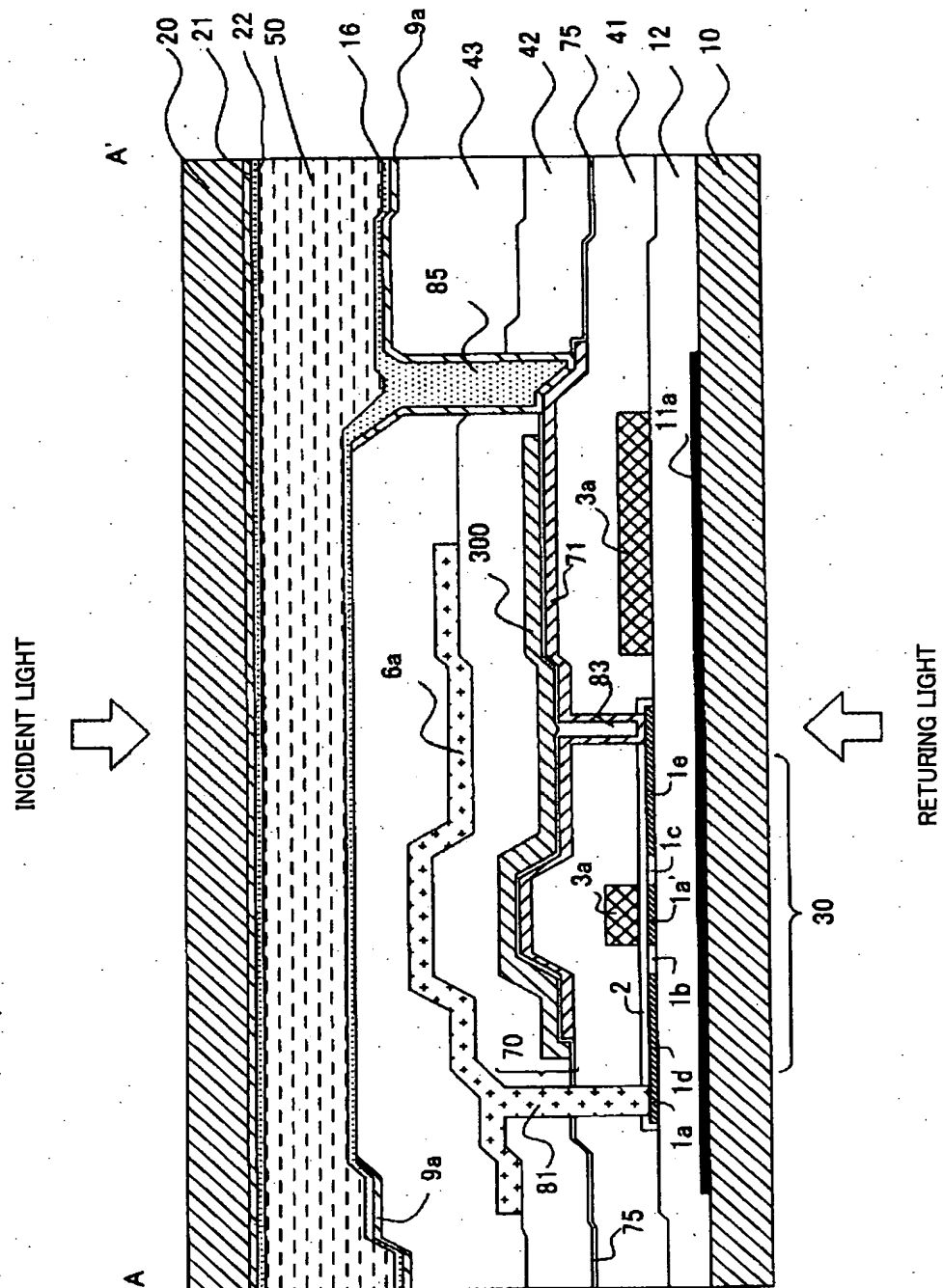


FIG. 5



A cross-sectional view of a semiconductor device 200. The device is built on a substrate 10, which is covered by a layer 12. Two gate electrodes 11aP are formed on the surface of layer 12. Above the gate electrodes, a layer 202 is formed, which contains a central region 203a. The top surface of the device is covered by a layer 206a. A channel region CH is located within the layer 202, directly above the gate electrodes 11aP. The device is labeled with various reference numerals: 10, 12, 11aP, 202, 203a, 206a, and CH. The entire structure is designated by the reference numeral 200.

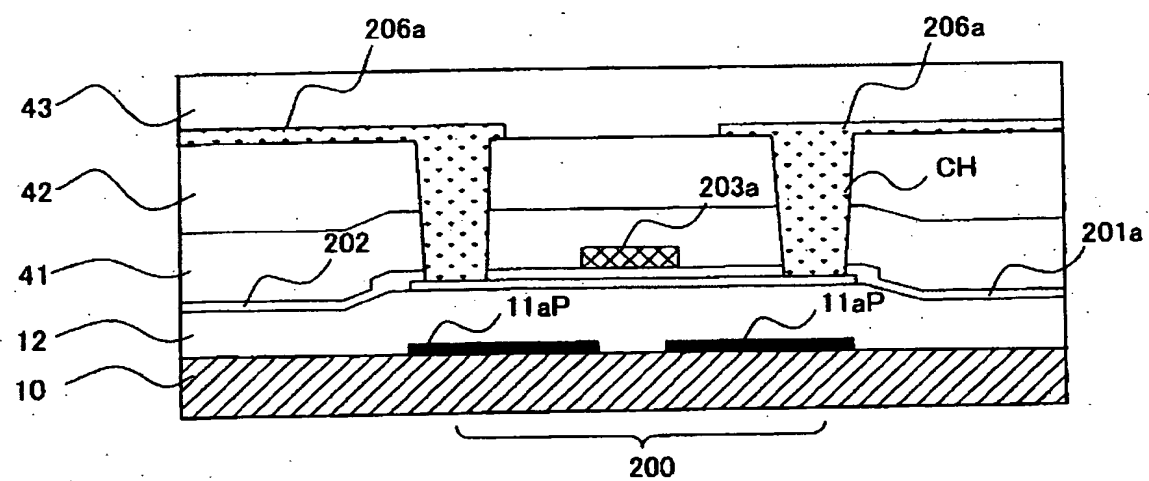


FIG. 7

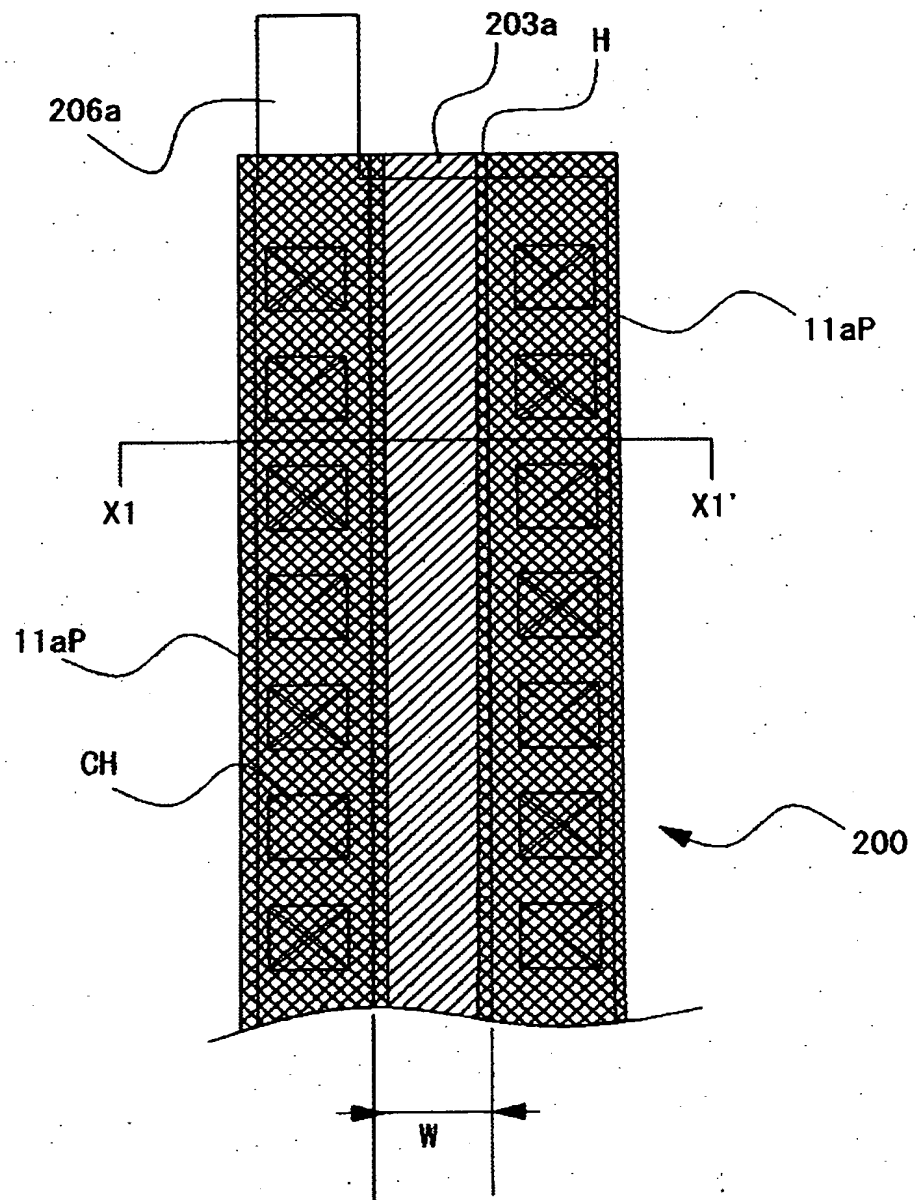


FIG. 8

X1

X1'

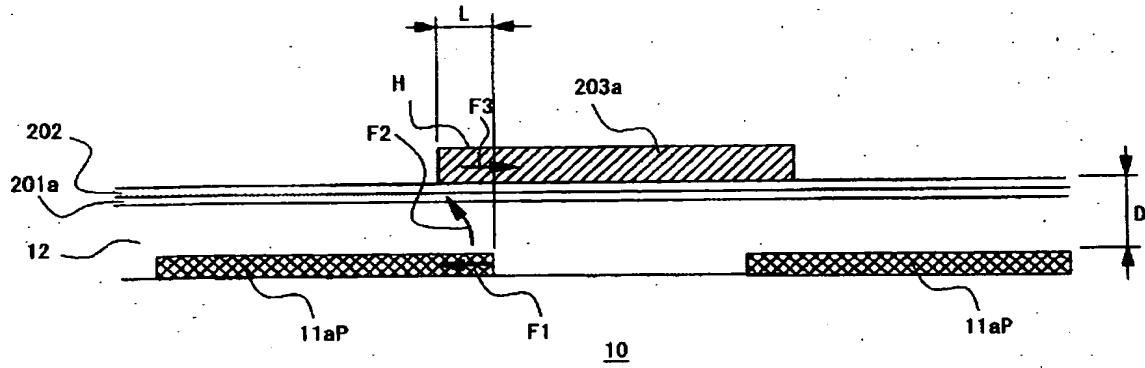


FIG. 9

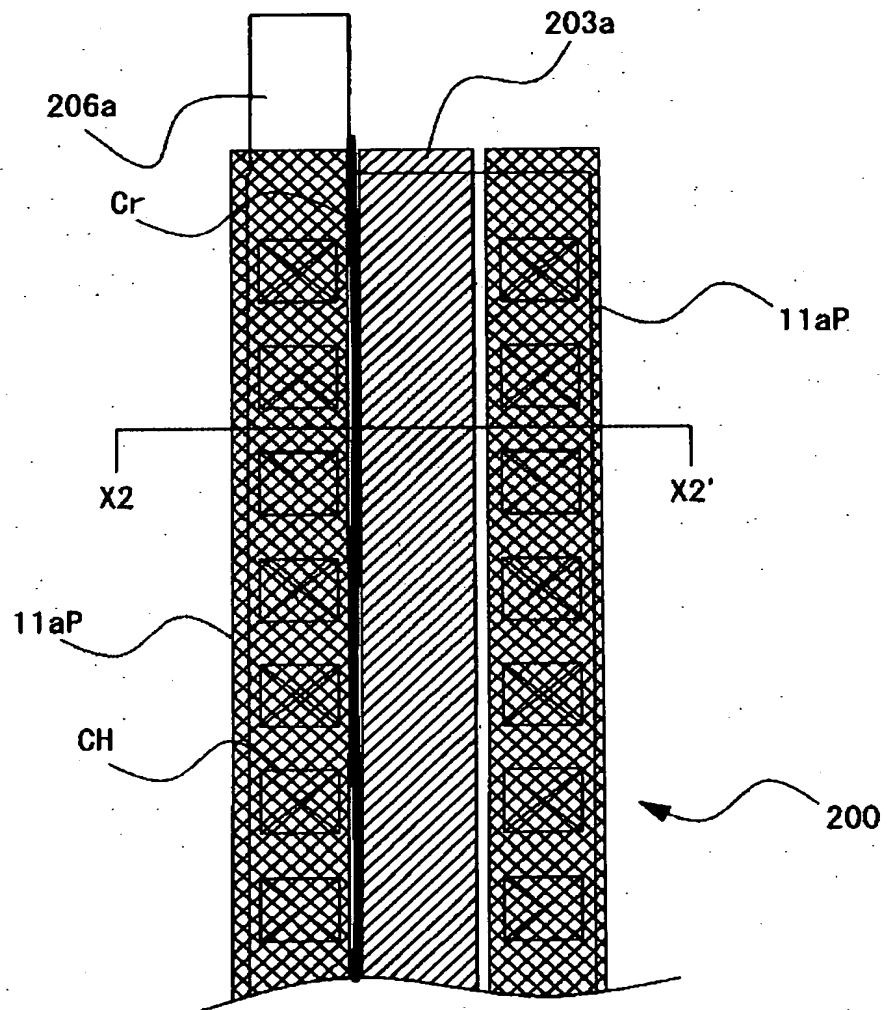


FIG. 10

X2

X2'

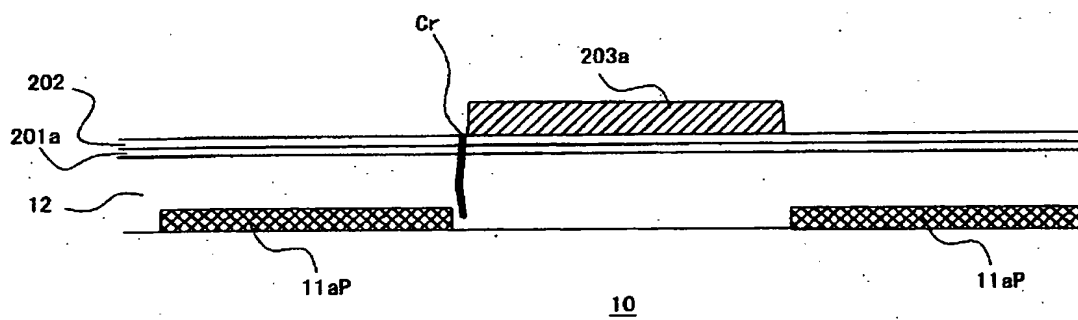


FIG. 11A

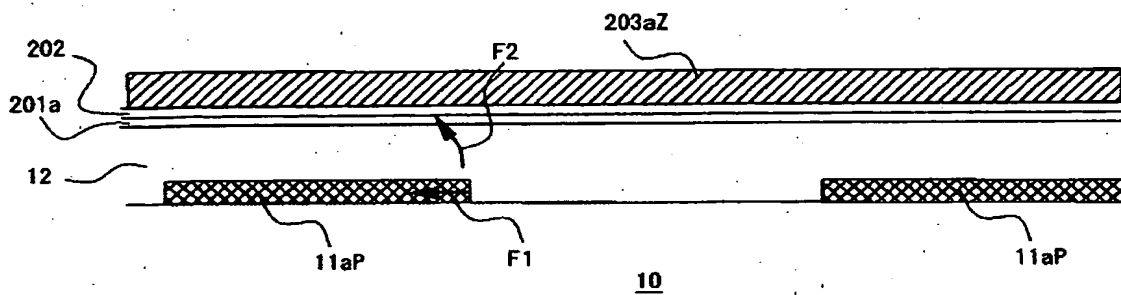


FIG. 11B

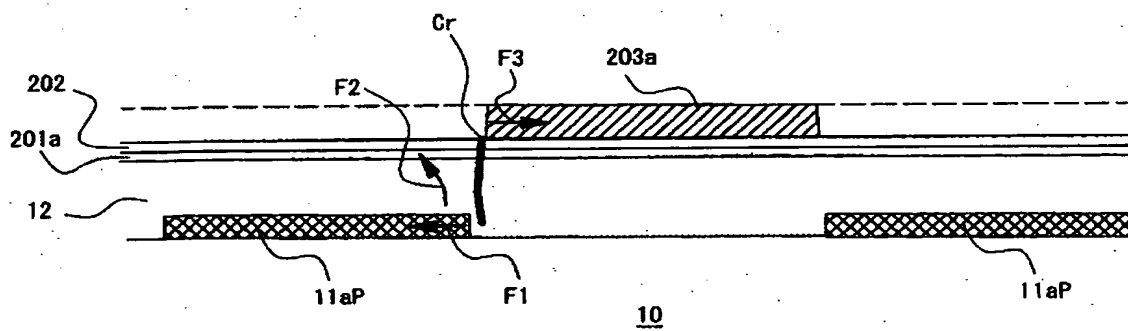


FIG. 12

